REMARKS

The Examiner has maintained the rejection of Claims 1-29 under 35 U.S.C. 102(e) as being anticipated by Migdal et al. (PN 6,426,753), hereinafter "Migdal." Applicant respectfully disagrees with this assertion.

Specifically, the Examiner now relies on the following excerpt from Migdal to show applicant's claimed "sending an instruction request to memory utilizing a texture module in a graphics pipeline" and "receiving instructions from the memory in response to the instruction request utilizing the texture module in the graphics pipeline."

> "10. A graphics subsystem for a computer system having a distributed text memory architecture, said graphics subsystem comprising:
>
> a) a texture request generator that generates texture requests and maps said texture requests to a plurality of cache addresses, wherein said texture requests are sent to distributed texture memories of said computer system according to a first ordering;
>
> b) an address queue for receiving and storing said plurality of cache addresses according to said first ordering;
>
> c) a cache memory for receiving texture responses from said distributed texture memories, wherein said texture responses enter said cache memory according to a second ordering; and
>
> d) a texture filter for performing texture filtering by retrieving said texture responses from said cache memory in an order corresponding to said first ordering and independent of said second ordering." (col. 14, lines 50-65)

The Examiner continues by stating that Migdal teaches a texture request being sent to distributed texture memories of a computer, and cache memory for receiving texture responses from distributed texture memories. Further, the Examiner asserts that, in a computer system, there are always instructions to input, output and process data (instruction request).

With respect to the Examiner statement regarding what is "always ... in a computer system," it appears that the Examiner has simply invoked Official Notice regarding applicant's claimed "instruction" limitation in the context of the remaining limitations. In response, applicant formally requests a specific showing of the subject matter in ALL of the claims. Note excerpt from MPEP below.

> "If the applicant traverses such an [Official Notice] assertion the examiner should cite a reference in support of his or her position." See MPEP 2144.03.

Even if the Examiner made such a showing, however, applicant contends that it would not be obvious to modify Midgal to include applicant's claimed "instruction request" and "instruction."

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

This criteria has simply not been met by the Examiner's rejection. Specifically, only applicant teaches and claims sending "instructions requests" and retrieving "instructions" in the specific context of "utilizing a texture module." By retrieving the instructions utilizing the texture module, much pipeline bandwidth is saved at the input of the texture module, since prior art configuration data at least in part need not necessarily be received from the rasterizer. Moreover, the memory traditionally employs a high-bandwidth connection with the texture module, which may be used for efficient retrieval of the instructions.

The instructions may then be used by the texture module in order to control various graphics processing involving the texels, pixels, and/or primitives, etc. For

example, the instructions may control how subsequent texels may be mapped to pixels associated with primitives. Moreover, the instructions may be used to control the mapping, or blending, of the texels with the pixels, in accordance with the instructions. Simply nowhere in the prior art is there such a combination of features for fulfilling the foregoing objectives.

Regarding Claims 6, 9, 18, and 19; it appears that the Examiner has simply dismissed applicant's previous remarks. Again, the subject matter of such claims further distinguishes various aspects of applicant's claimed "instruction"-type limitations from the prior art. More importantly, the aforementioned anticipation criteria has simply not been met by the Examiner's rejection.

For example, applicant claims that "the instructions are adapted for controlling a texture environment module coupled to the texture module" (see Claim 6). The Examiner relies on col. 5, lines 15-20 of Migdal to show such feature in the prior art. See below.

> "The G chip 105 accepts instructions and data from Crosstalk streams 106. The instructions are executed by microprocessor 103 and G chip 105. G chip 105 also performs geometric calculations on vertex data. Data is temporarily cached in SRAM 104. Eventually, the resulting vertex data is sent over the high bandwidth network 102 to one of the R subsystems." (col. 5, lines 15-20)

After a careful review, applicant contends that such excerpt is lacking, especially in view of the shortcomings of the Examiner's application of Migdal to the independent claims. For example, the abovementioned "microprocessor" and "G chip" do not include a "texture module," as claimed by applicant. Only applicant teaches and claims sending "instructions requests" and retrieving "instructions" "utilizing a texture module" which provides the aforementioned advantages that are non-existent in the prior art including Migdal. Thus, the aforementioned anticipation criteria has simply not been met by the Examiner's proposed excerpt.

Similarly, applicant claims that "the initial instructions control at least the sending of the instruction request by the texture module" (see Claim 9), "a complete

instruction set is received in response to the instruction request" (see Claim 18), and "a partial instruction set is received in response to the instruction request" (see Claim 19). The Examiner relies on the following excerpts from Migdal to show such features in the prior art.

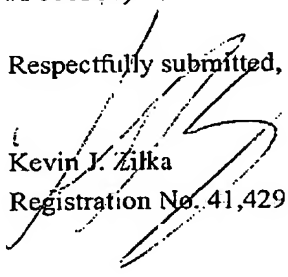
> "As stated above, the R chip 501 accepts geometric and pixel primitives from the network and renders each one into a specified 16.times.16 screen patch. The R chip 501 also handles requests from other R chips for texture data and requests from the display subsystem for frame buffer data. Attached to this are sixteen M (multisample) memory chips, which are used to store the frame buffer screen patches corresponding to the subsystem." (col. 7, lines 55-60)

> "Texture request generator 603 also maps the texture coordinates to a cache address and sends the cache address to FIFO memory 604, which acts as a queue for cache addresses. Cache addresses received by FIFO memory 604 will reach texture filter 605 after multiple clock cycles. Texture filter 605, upon receiving the cache addresses, will retrieve the texture responses from the texture response buffer 608." (col. 9, lines 30-37)

Again, the aforementioned anticipation criteria has simply not been met by the Examiner's reference. A specific prior art showing of such claim limitations or a notice of allowance is respectfully requested. All of the pending independent claims are thus deemed allowable along with any claims depending therefrom.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP064/P000286).

Respectfully submitted,



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